

## REMARKS

The present application was filed on December 21, 2001 with claims 1-18. Claims 1-18 remain pending. Claims 1 and 18 are the independent claims.

Claims 1-6, 8-12 and 15-18 stand rejected under 35 U.S.C §102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0087709 (hereinafter “Kerr”). The remaining claims stand rejected under 35 U.S.C. §103(a) over Kerr in combination with other cited references.

In this response, Applicants respectfully traverse the §102(e) and §103(a) rejections, and amend independent claims 1 and 18.

With regard to the §102(e) rejection, Applicants initially note that MPEP §2131 specifies that a given claim is anticipated “only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference,” citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the “identical invention . . . in as complete detail as is contained in the . . . claim,” citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For the reasons identified below, Applicants submit that the Examiner has failed to establish anticipation of claims 1-6, 8-12 and 15-18 by Kerr.

Independent claims 1 and 18 as originally filed recite the directing of packets to one or more operational units in a manner that maintains a desired function call sequencing over one or more packets for one or more order-dependent processing tasks. Such an arrangement provides significant advantages in terms of improving processor throughput. See the specification at, for example, page 1, line 25, to page 2, line 15, and page 3, lines 11-12.

It is believed that Kerr fails to teach or suggest the claimed arrangements, and fails to provide their associated processor throughput advantages.

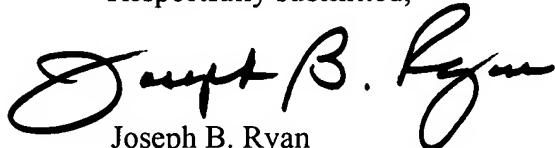
In formulating the §102(e) rejection, the Examiner relies on step 204 of FIG. 8 and step 604 of FIG. 10 in Kerr as allegedly disclosing the above-noted claim limitations relating to maintenance of a desired function call sequencing. However, the relied-upon portions of Kerr, and the associated textual description, do not make any mention whatsoever regarding function calls, much less the claimed maintenance of a particular sequence of such function calls.

Accordingly, the §102(e) rejection is believed to be improper, and should be withdrawn. The additional references fail to supplement the above-noted fundamental deficiencies of Kerr as applied to the independent claims, and the §103(a) rejections are therefore also believed to be improper and should be withdrawn.

Notwithstanding the traversal, Applicants have amended claims 1 and 18 without prejudice, solely in order to expedite prosecution of the application. More specifically, Independent claim 1 has been amended to specify that the control circuitry comprises ordering logic having at least one ordering queue and at least one configuration register. One possible example of an arrangement of this type is shown and described in the present application in conjunction with the illustrative embodiment of FIG. 3. The ordering queue stores identification information used to maintain the desired function call sequencing for a designated set of functions, and the configuration register stores information specifying that set of functions. See the specification at, for example, page 6, line 25, to page 13, line 25. A similar amendment has been made to independent claim 18.

In view of the above, Applicants believe that claims 1-18 are in condition for allowance, and respectfully request the withdrawal of the §102(e) and §103(a) rejections.

Respectfully submitted,



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